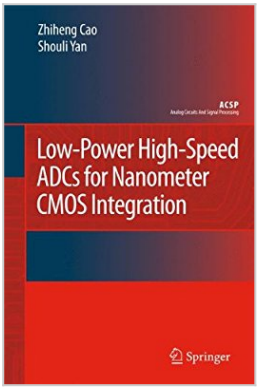

Low-Power High-Speed ADCs for Nanometer CMOS Integration (Analog Circuits and Signal Processing)

By Zhiheng Cao, Shouli Yan

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Low-Power High-Speed ADCs for Nanometer CMOS Integration is about the design and implementation of ADC in nanometer CMOS processes that achieve lower power consumption for a given speed and resolution than previous designs, through architectural and circuit innovations that take advantage of unique features of nanometer CMOS processes. A phase lock loop (PLL) clock multiplier has also been designed using new circuit techniques and successfully tested.

1) A 1.2V, 52mW, 210MS/s 10-bit two-step ADC in 130nm CMOS occupying 0.38mm^2. Using offset canceling comparators and capacitor networks implemented with small value interconnect capacitors to replace resistor ladder/multiplexer in conventional sub-ranging ADCs, it achieves 74dB SFDR for 10MHz and 71dB SFDR for 100MHz input.

2) A 32mW, 1.25GS/s 6-bit ADC with 2.5GHz internal clock in 130nm CMOS. A new type of architecture that combines flash and SAR enables the lowest power consumption, 6-bit >1GS/s ADC reported to date. This design can be a drop-in replacement for existing flash ADCs since it does require any post-processing or calibration step and has the same latency as flash.

3) A 0.4ps-rms-jitter (integrated from 3kHz to 300MHz offset for >2.5GHz) 1-3GHz tunable, phase-noise programmable clock-multiplier PLL for generating sampling clock to the SAR ADC. A new loop filter structure enables phase error preamplification to lower PLL in-band noise without increasing loop filter capacitor size.

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Editorial Review

From the Back Cover

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